Rapid Prototyping on a Structured ASIC Fabric

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Abstract – We describe the architecture of a structured ASIC fabric in which the logic and routing can be customized using three masks. A standard Cadence based design flow is employed, and using an active dynamic backlight controller as an example, performance is compared to that of an ASIC implementation in the same technology.

I Introduction

As non-recurrent engineering costs for ASICs continue to increase, structured ASICs (SASICs) which allow the reuse of mask sets will gain in importance. Logic cell design has a major impact on the performance of such fabrics and in this work a transmission gate based cell with programmable driving strength is described. Although other SASIC designs have been reported, many did not consider practical issues such as design tool integration, buffer insertion, clock tree generation and filler cells. Our SASIC library is created for a timing-driven P&R flow and adopts a fine-grained cell design. In contrast, most academic publications focus on using FPGA-like CAD flows. Test chip TO-1 (Fig. 1) was used to compare three logic cell designs: the complementary universal logic gate, complementary transmission gate (TG) and single ended TG [1]. For the work described in this paper, the TG scheme was selected as it had the best speed and power consumption, and used to implement test chip TO-2, an active dynamic backlight controller [2] in UMC 0.13um 1 poly 8 metal layer CMOS technology.

II. Cell and Library Design

A synchronous digital circuit contains both logic and storage elements. In our design, 3-input lookup tables (3-LUT) are used for combinatorial logic and dedicated universal flip-flops with scan support for sequential logic. The 3-LUT has a logic equivalent of approximately 2 two-input NAND gates. A logic block is made from eight lookup tables and a flip-flop. The resulting gate array-like organisation is shown in Fig 2.

A structured ASIC cell library is implemented using Cadence Virtuoso, and simulated with Encounter Library Characterizer (ELC) and the Spectre mixed-signal simulator. A library consisting of one type of D flip-flop and programmable 3-LUTs is created. The regularity of the cell design and a small number of cell types simplified development of the fabric, yet supports all digital ASIC functions, including latches, tri-state buffers and gated-clock cells. The layout of 3-LUT is shown in Fig 3 and can be customized to be either a TG-based function generator or a programmable buffer. The function generator can implement 76 unique 2-input or 3-input logical functions. The buffer provides 3 different drive strengths (1x, 1.67x, 3.33x). A single metal layer, M3 connects the fixed vias to customize the function generator and select the buffer strength. The 3-LUT can also be configured as a filler cell and act as a supply rail decoupling capacitor. To fulfill the power budget of high speed applications, dedicated horizontal and vertical strips are implemented in cell layout efficiently.

MCNC benchmarks and real applications (H.264 codec and 8 to 32bit MCU) are studied. Our study shows that 3 output driving strengths are sufficient to support most applications with aggressive performance constraints. All benchmarks can be routed in our fabric with 2 metal layers, M3 (50% availability) and M4. Routing congestion is alleviated by assigning the logic customization vias in a manner to minimize blocking of the routing channels. Cell schematics, layout, simulation model, timing model are generated and qualified with Cadence software and the SASIC design environment is exactly the same as for ASICs.

The application design is mapped to our fabric as follows. First, the target application coded in register transfer language (RTL), is synthesized using our library with Synopsys DC Compiler. Next, the gate netlist is placed and routed by Cadence Encounter assisted by our custom legalization script which places the storage elements in pre-defined regions. The remaining steps follow the standard ASIC design flow.

The computationally intensive part of an active dynamic backlight controller is extracted and mapped to our fabric. The design computes the LED brightness at 180 small regions of a 1.5Gbps full HD 1080p resolution video frame. The simulated output of TO-2 is shown in Fig 4. TABLE I shows the comparison between the implementations of TO-2 based on our structured ASIC library and ASIC library. TABLE II gives a summary of the key TO-2 features.

III. Results

TO-2 (Fig 5) consists of 1578 LUTs, 106 flip-flops and 56 IO pins. It utilizes 19% of MPW area and operates at 83MHz. Our fabric achieves ~85% of the speed and ~3.5 times the area of a standard cell based ASIC implementation.

V. Conclusion

A metal programmable SASIC with full ASIC CAD tool compatibility has been described. A video processing application chip is fabricated and passed the scan test and functional test successfully. Performance of the SASIC is verified and similar to an ASIC with an area penalty factor of 3.5.

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References

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[2] Peng, et al., High Contrast LCD TV Using Active Dynamic LED Backlight, SID Symposium Digest of Technical Papers, Volume 38, Issue 1, pp. 1336-1338, May 2007.

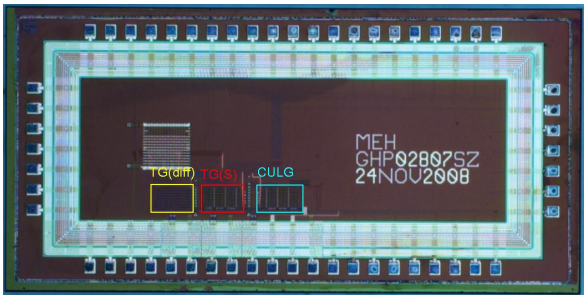

Fig 1. Test chip (TO-1) micrograph with metal 6 exposed

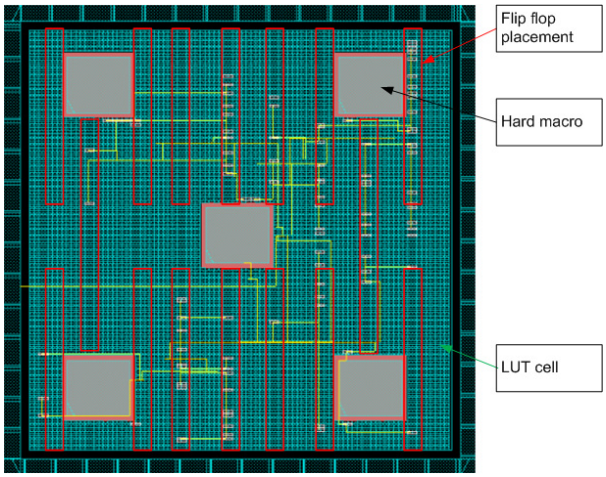

Fig 2. Cell organisation of a gate array-like fabric with ratio of FF to LUT (1:8) and five memory macros

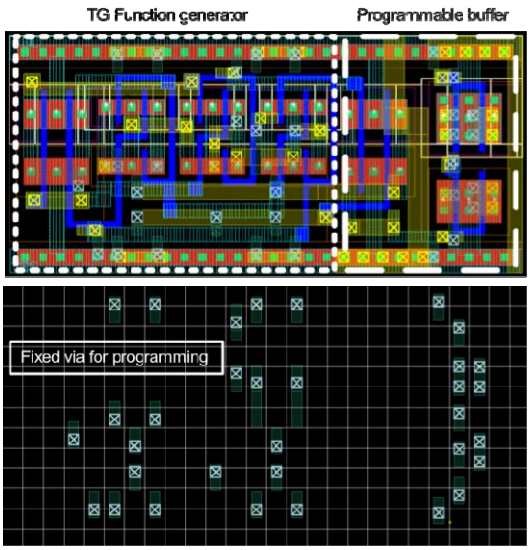

Fig 3. Layout of programmable 3-LUT

Fig 4. A sample image of the target application with a high definition still picture (1080p) is shown. The insert in the top-left corner shows the (output) brightness of the LED backlight panel.

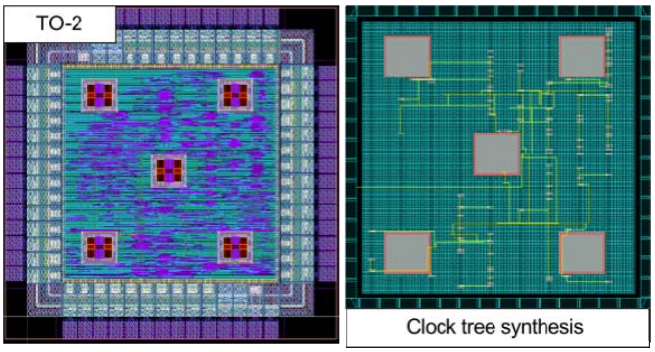

Fig 5. Screen capture of TO-2
(Left: topview; Right: Clock tree synthesis)

TABLE I
Comparison between our fabric and ASIC implementation of TO-2

	Our fabric	**ASIC**
Area (sq. mm)	0.157	0.045
Max. operating frequency (MHz)	100	118
Density (per sq. mm)	20 KLUT	250 Kgate
Chip density (utilization)	82%	80.5%
Routing layers	2 (M3-M4)	3 (M2-M4)
Number of mask for change of design	3	All

TABLE III
TO-2 design summary

	Our fabric	**Unit**
Equivalent gate count (2-input NAND)	3571	gate
Size of LUT	49.92	sq. um
Transistor count at LUT	24	gate
Dual port memory (32 x 8bit) used	1 of 5	unit
Chip size (pad-limited)	1.5 x 1.5	sq. mm